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TO:	FROM:
Board of Patent Appeals and Interferences [Examiner Te Y. CHEN]	Jeffrey R. Joseph

COMPANY:	DATE:
USPTO	May 7, 2007

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RE:	YOUR REFERENCE NUMBER:
Serial No.: 10/659,133	Group Art Unit: 2161

☐ URGENT   ■ FOR REVIEW   ☐ PLEASE COMMENT   ☐ PLEASE REPLY   ☐ CONFIRMATION

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Notes/Comments: **REPLY BRIEF**

1. Fax Cover Sheet (1)
2. Reply Brief (_4_)
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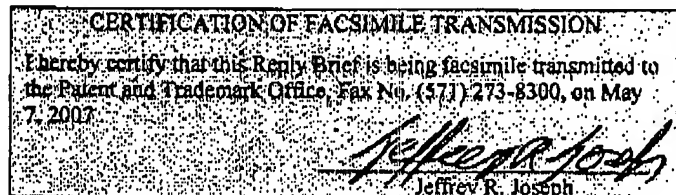CENTRAL FAX CENTER
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Patent

Attorney Docket No.: Intel 2207/618602
Assignee: Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS   :   Per HAMMARLUND et al.   CONFIRMATION NO.: 4796

SERIAL NO.   :   10/659,133

FILING DATE   :   September 10, 2003

GROUP ART UNIT :   2161

FOR   :   ACCESS CONTROL OF A RESOURCE SHARED BETWEEN COMPONENTS

EXAMINER   :   Te Y CHEN

M/S: APPEAL BRIEFS – PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATION OF FACSIMILE TRANSMISSION
I hereby certify that this Reply Brief is being facsimile transmitted to the Patent and Trademark Office, Fax No. (571) 273-8300, on May 7, 2007.

Jeffrey R. Joseph

ATTENTION: Board of Patent Appeals and Interferences

REPLY BRIEF

Dear Sir:

This Reply Brief is submitted in response to the Examiner's Answer mailed in this case on March 6, 2007.

Appellants submit this Reply Brief to address issues raised in the Examiner's Answer.

Application No.: 10/659,133
Filing Date: September 10, 2003
Appellant(s): Per Hammarlund et al.
Reply Brief Filed: May 7, 2007

REMARKS

Claims 2-11, 13, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ebrahim et al. (USP 5,644,753) in view of Arimilli et al. (USP 5,867,511). Apellants' independent claim 2 recites in part: "access to the partitioned elements by said first and second components is controlled based on said first mask value . . . ." Examiner cites the following portion of Ebrahim as teaching this element of claim 2:

> The first mode of operation is used for all access requests by the data processor and for system controller access requests when the mode flag has a first value. The second mode of operation is used for the system controller access requests when the mode flag has a second value distinct from the first value.

See Ebrahim Abstract. The Examiner, however, fails to provide the portion of the abstract that describes the first and second modes.

> The cache controller has two modes of operation, including a first standard mode of operation in which read/write access to the cache memory is preceded by generation of the hit/miss signal by the comparator, and a second accelerated mode of operation in which read/write access to the cache memory is initiated without waiting for the comparator to process the access request's address value.

In Ebrahim, the two modes distinguish between what does or does not happen <u>before</u> accessing the cache. <u>Access</u> is not <u>controlled based on</u> the mode flag.

Even assuming, *arguendo*, that the mode flag can be viewed as a mask value as claimed by Appellants, Examiner's argument still fails to read Ebrahim onto Apellants' claimed invention. On page 11 of the Examiner's Answer, Examiner asserts that "the system controller and the data processor definitely represent the claimed first and second components . . . ." According to the Ebrahim reference:

> The access circuitry uses the first mode of operation for all access requests by the data processor coupled to the cache memory and for access requests by the system controller when the mode flag has a first value. It uses the second mode of operation for access requests by the system controller when the mode flag has a second value distinct from the first value.

Ebrahim at 4:33-39. This portion of Ebrahim makes it clear that the mode flag only affects the mode of the system controller, while the data processor always operates in the first mode.

Apellants' independent claim 2 states that "wherein access to the partitioned elements by said first and second components is controlled based on said first mask value." Emphases added.

On page 11 and 12 of the Examiner's Answer, the Examiner rehashes her argument about the UPANUM field teaching the first mask value of Apellants' claimed invention. Apellants' reiterate that the only description in the Ebrahim reference regarding the UPANUM field states that it "is a 5-bit mask field that specifies the maximum number of UPA ports the System Controller can support." Ebrahim 22:8-10. In both her Answer and the previous Office Actions, Examiner fails to explain how specifying the maximum number of UPA ports teaches "wherein access to the partitioned elements by said first and second components is controlled based on said first mask value."

CONCLUSION

In view of the above, Appellants respectfully submit that the rejection of claims 2-11, 13, 18 and 20 should be reversed. Appellants therefore respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's decision rejecting claims 2-11, 13, 18 and 20 and direct the Examiner to pass the case to issue.

The Examiner is hereby authorized to charge any additional fees which may be necessary for consideration of this paper to Kenyon & Kenyon LLP Deposit Account No. 11-0600.

SJ01 101455 v1

Application No.: 10/659,133
Filing Date: September 10, 2003
Appellant(s): Per Hammarlund et al.
Reply Brief Filed: May 7, 2007

Respectfully submitted,

KENYON & KENYON LLP

Date: <u>May 7, 2007</u>   By: _____

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